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	APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
	10/678,533	10/03/2003	Steven M. Havlik	H0004388US	1324
	7:	7590 01/12/2005		EXAMINER	
	Honeywell International, Inc.			PHILOGENE, HAISSA	
		Patent Services Group			
101 Columbia Road		Road		ART UNIT	PAPER NUMBER
	Morristown, NJ 07962			2828	
			DATE MAILED: 01/12/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

		M·H					
	Application No.	Applicant(s)					
Office Action Summan	10/678,533	HAVLIK ET AL.					
Office Action Summary	Examiner	Art Unit					
	Haissa Philogene	2828					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1) Responsive to communication(s) filed on <u>03 O</u>	ctober 2003.						
	action is non-final.						
3) Since this application is in condition for allowar	<u></u>						
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4)⊠ Claim(s) <u>1-30</u> is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) 10-16 is/are allowed.							
6) Claim(s) 1-3,8,9,17-19,24-27,29 and 30 is/are	6)⊠ Claim(s) <u>1-3,8,9,17-19,24-27,29 and 30</u> is/are rejected.						
7) Claim(s) <u>4-7,20-23 and 28</u> is/are objected to.	<u> </u>						
	8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers							
9) ☐ The specification is objected to by the Examiner.							
10)⊠ The drawing(s) filed on <u>03 October 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) □ All b) □ Some * c) □ None of:							
1. Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No							
3. Copies of the certified copies of the priority documents have been received in this National Stage							
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.							
Attachment(s)							
1) Notice of References Cited (PTO-892)	4) 🔲 Interview Summary	(PTO-413)					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail D	ate					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Informal F 6) Other:	Patent Application (PTO-152)					



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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 8, 9 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitani et al., Patent No. 6,731,871.

As per claims 1 and 25, Kitani discloses in Fig.1 a LED driver circuit and method thereof comprising:

a voltage booster (13) coupled to receive an input voltage Vbat and coupled to provide an output voltage having an increased magnitude (3.3 V) relative to the input voltage; a current source (5a, 6, 7) coupled to receive the input voltage and to provide a substantially constant current in response to the input voltage when the transistor 7 is switched ON by an instruction from the controller 1 (see Col.1, lines 56-60); and a component (5a) coupled to the voltage booster (13) and the current source (5a, 6, 7), wherein the voltage booster (13) as a driver activates the component (5a) using the output voltage and the substantially constant current.

As per claims 8 and 9, Kitani discloses the component (5a) including a light emitting diode (LED) having an illumination state controlled by the voltage booster (13); a



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forward current If conducted by the LED (5a) being substantially equal to the substantially constant current (see Col.1, lines 56-60 and Col.2, lines 21-25).

Claims 1-3, 8, 9, 25-27, 29 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Worley, Sr. et al., Patent No. 6,486,726.

As per claims 1 and 25, Worley discloses in Figs.2, 3 and 7A a LED driver circuit and method thereof comprising: a voltage booster (215 or 305-322) coupled to receive an input voltage Vdd and coupled to provide an output voltage having an increased magnitude (217 or 327) relative to the input voltage; a current source (715-735) coupled to receive the input voltage via oscillator 305 and to inherently provide a substantially constant current in response to the input voltage upon setting; and a component (205 or 705, 710) coupled to the voltage booster and the current source, wherein the voltage booster activates the component using the output voltage and the substantially constant current upon enablement by an input buffer 225 to turn ON the LED component 205 when it receives a high level logic signal.

As per claims 2, 3, 26 and 27, Worley discloses the voltage booster comprising a buffer (225) when receiving a high level logic signal 222, in a pull operation, coupled to cause a charging signal (220) in response to a first polarity (positive) of the input voltage (Vdd); and an energy storage device (320) coupled to receive the charging signal via charge pump (215, or 305-322) to increase a voltage developed across the energy storage device 320; said buffer (225) being further coupled to cause a driving signal by the inverter (310), in a push operation, in response to a second polarity (ground



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potential) of the input voltage, the driving signal being combined with the voltage developed across the energy storage device (320) to produce the output voltage (2 Vdd). See also Col.6, line 14 – Col.7, lines 2 and 22-30.

As per claims 8 and 9, Worley discloses the component (205 or 705,710) including a light emitting diode (LED) having an illumination state controlled by the voltage booster (215 or 305-322); a forward current If conducted by the LED (5a) being substantially equal to the substantially constant current since the current regulator (715-735) is used to set the current flowing into the LED.

As per claims 29 and 30, Worley discloses a Light Emitting Diode (LED) control circuit, comprising: means (210, 315, 327) for charging an energy storage device (320) during a first phase of operation of the LED control circuit, i.e. when switched to the low output state by the pulsing signal of the oscillator 305, the inverter 310 pulls the low electrode 322 of the capacitor 320 down to ground; and means (310, 322, 327) for discharging the energy storage device C during a second phase of operation of the LED control circuit to illuminate an LED (205), i.e., when switched to the high output state by the pulsing signal, the inverter raises the voltage at the low electrode of the capacitor to Vdd, which causes the voltage at the high electrode 327 of the capacitor to rise above Vdd-Vt, said high electrode rises until it reaches the turn ON voltage of the LED approaching 2 Vdd-Vt (see Col.6, line 45- Col.7, lines 2 and 22-30), wherein means for discharging the energy storage device comprises: means (215 or 305-327) for summing the charge stored in the energy storage device with an illumination signal as control logic signal received upon enablement of the input buffer 225; and means (715-735) for supplying a



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constant current during the second phase of operation which is approximately equal to the current being supplied to the low electrode 322 of the capacitor 320 from the inverter 310; wherein the means for summing the charge stored comprises means (315) for inherently blocking the power supply when reverse biased to induce a control voltage greater than a magnitude of the power supply provided by inverter 310 and capacitor 320.

Claims 1-3, 8, 9 and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Horiuchi et al., Pub. No. 2004/0195978.

As per claims 1 and 25, Horiuchi discloses in Fig.1 a driver circuit and method of controlling a luminescent state of a LED, comprising:

a voltage booster (27) coupled to receive an input voltage Vdd and coupled to provide an output voltage having an increased magnitude (Vh (9V)) relative to the input voltage; a current source (12-14) coupled to receive the input voltage via control circuit 11 and to provide a substantially constant current in response to the input voltage; and a component (21-26) coupled to the voltage booster (27) and the current source (12-14), wherein the voltage booster (27) activates the component (21-26) using the output voltage and the substantially constant current.

As per claims 2, 3, 26 and 27, Horiuchi discloses in Fig.1 the voltage booster (27) comprising the control circuit 11 generating a signal Cont to perform ON-OFF control of the control switch Q27 readable as a buffer coupled to provide a charging signal (see page 3, Col.2, lines 32-37) in response to a first polarity (positive) of the input voltage (Vdd); and an energy storage device (C27) coupled to receive the charging signal to



increase a voltage developed across the energy storage device; said buffer being further coupled to cause a driving signal via constant-current driver 12 in response to a second polarity (ground potential) of the input voltage (Vdd), the driving signal being combined with the voltage developed across the energy storage device (C27) via ground to produce the output voltage (Vh(9V)).

As per claim 8, Horiuchi discloses the component (21-26) including a light emitting diode (LED) having an illumination state controlled by the voltage booster (27). As per claim 9, Horiuchi discloses in Fig.2 a forward current If conducted by the LED being substantially equal to the substantially constant current (20 mA) (see also page 3, Col.2, lines 53-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 17-19 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dushane et al., Patent No. 6,116,512, in view of Horiuchi et al.

As per claim 17, Dushane discloses in Figs.1 and 3 an environmental control system (20, see Col.4, lines 66-67), comprising: a display controller (54) coupled to the environmental control system (20) to provide display information; a thermostat (20) comprising an LCD (38, 66) coupled to receive the display information (see Col.3, lines 52-54), and an LCD backlight system (52) coupled to the LCD. Dushane does not



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disclose the LCD backlight system comprising: a voltage booster coupled to receive a lighting control signal and coupled to provide an output signal having an increased magnitude of the lighting control signal; a current source coupled to receive the lighting control signal and coupled to provide a substantially constant current in response to the lighting control signal; and a Light Emitting Diode (LED) coupled to the voltage booster and the current source, wherein the voltage booster activates the LED using the output signal and the substantially constant current. Horiuchi discloses a LCD backlight system comprising a voltage booster (27) coupled to receive a lighting control signal (Cont) from a control circuit 11 and coupled to provide an output voltage having an increased magnitude (Vh (9V)) of the lighting control signal; a current source (12-14) coupled to receive a control signal (S1-S3) from the control circuit 11 and coupled to provide a substantially constant current in response to the control signal; and a LED (21-26) coupled to the voltage booster (27) and the current source (12-14), wherein the voltage booster (27) activates the LED (21-26) using the output voltage and the substantially constant current. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the LCD backlight system as taught by Horiuchi into the Dushane type environment control system, because it would allow the use of low voltage ICs and minimization of the power consumption, thereby improving the efficacy of the system.

As per claims 18, 19 and 24, Dushane in view of Horiuchi et al. discloses the claimed invention substantially as explained above. Further, Horiuchi discloses the voltage

booster comprising: the control circuit 11 generating a signal Cont to perform ON-OFF control of the control switch Q27 readable as a buffer coupled to provide a charging signal (see page 3, Col.2, lines 32-37) in response to a first polarity (positive) of the lighting control signal (Cont); and an energy storage device (C27) coupled to receive the charging signal to increase a voltage developed across the energy storage device; said buffer being further coupled to provide a driving signal via constant-current driver 12 in response to a second polarity (ground potential) of the lighting control signal, the driving signal being combined with the voltage developed across the energy storage device (C1) via ground to produce the output signal (Vh(9V)). In addition, Horiuchi discloses in Fig.2 a forward current If conducted by the LED being substantially equal to the substantially constant current (20 mA) (see also page 3, Col.2, lines 53-60).

Allowable Subject Matter

Claims 4-7, 20-23 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art fails to disclose that the current source comprises:

a bias generation circuit coupled to provide a bias voltage in response to the input voltage or lighting control signal; and a current conduction device coupled to receive the bias voltage and coupled to provide the substantially constant current in response to the bias voltage (claims 4 and 20); that the step of generating a substantially constant current comprises: forming a bias signal in response to the

second phase of the input signal; and inducing a conductive state of a current control device in response to the bias signal, wherein the substantially constant current is proportional to the bias signal (claim 28).

Claims 10-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to disclose a method of controlling backlighting associated with a display having the steps of: storing charge from a power source in a first phase of operation when a bias voltage supplying at least one Light Emitting Diode (LED) is less than a forward voltage required by the LED, wherein the power source provides a voltage level lower than the forward voltage required by the LED; in a second phase of operation, combining an operating voltage with the stored charge to illuminate the LED using the combined voltage as the bias voltage; and alternating the first and second phases of operation to control the backlighting associated with the display (claim 10).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Williams, Patent No. 6,680,834.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haissa Philogene whose telephone number is (571) 272-1827. The examiner can normally be reached on 6:30 A.M.-6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hp

Haissa Philogene Primary Examiner A. A.J., 28276, 6